PATENT ABSTRACTS OF JAPAN

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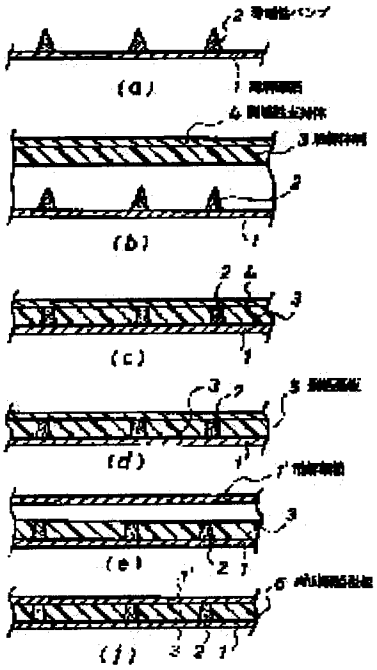
(54) MANUFACTURE OF MULTI-LAYER PRINTED BOARD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method for manufacturing a multi-layer wiring board with good yield and high reliability while the connection state between wiring pattern layers is visually observed with ease.
SOLUTION: A process where a conductive projection 2 is provided on one main surface of a conductor foil 1, a process where an insulator layer 3 of thermo-melting and thermo softening is formed on one main surface of a peeling supporter 4, a process where the peeling supporter 4 is provided in lamination on the formation surface of the conductive projection 2 of the conductor foil 1 with the insulator layer 3 faced, a process where the laminated body is processed under heat and pressure and the melted or softened insulator layer 3 is made to penetrate the tip end part of the conductive projection 2, which is hit to a facing peeling supporter 4 surface, a process where the peeling supporter 4 is peeled and removed so the tip end part of the conductive projection 2 which is insulated and separated from each other is exposed, a process where a conductor foil 1' is laminated at the exposed surface of the tip end part of the conductive projection 2, which is processed under heat and pressure for consolidation to form a conductor foil plated plate 6 of both-surface connection type, under process where the both-surface conductor foils 1 and 1' are wiring-patterned, are provided.



CLAIMS

[Claim(s)]
[Claim 1]A manufacturing method of a multilayer interconnection board characterized by comprising the following.
A process of providing conductive projections in the 1 principal surface of conductor foil.
A process of forming in the 1 principal surface of a detachability base material an insulation layer in which thermofusion thru/or heat softening is possible.
A process of making an insulation layer countering a conductive-projections forming face of said conductor foil, and carrying out lamination arrangement of the detachability base material.
A process which performs heat pressing processing to said layered product, makes a tip part of conductive projections **** and is made to opposite-** melting-izing thru/or a softened insulation layer to a detachability base material side which counters, A process at which a tip part of conductive projections which carry out the strip of said detachability base material, and carry out insulating isolation mutually is exposed, A process of carrying out lamination arrangement of the conductor foil, and performing heat pressing processing to an exposed surface of said conductive-projections tip part, uniting with it, and forming a front-back-connection type conductor foil tension board, and a process of carrying out wiring patterning of said double-sided conductor foil.

[Claim 2]A manufacturing method of the multilayer interconnection board according to claim 1, wherein conductor foil is electrolytic copper foil.
[Claim 3]A manufacturing method of a multilayer interconnection board characterized by comprising the following.
A process of providing conductive projections in a prescribed position of said circuit pattern of a core wiring board with which a circuit pattern is provided in the at least 1 principal surface.
A process of forming in the 1 principal surface of a detachability base material an insulation layer in which thermofusion thru/or heat softening is possible.
A process of making an insulation layer countering a conductive-projections forming face of said core wiring board, and carrying out lamination arrangement of the detachability base material.
A process which performs heat pressing processing to said layered product, makes a tip part of conductive projections **** and is made to opposite-** melting-izing thru/or a softened insulation layer to a detachability base material side which counters, A process at which a tip part of conductive projections which carry out the strip of said detachability base material, and carry out insulating isolation mutually is exposed, A process of carrying out lamination arrangement of the conductor foil, and performing heat pressing processing to an exposed surface of said conductive-projections tip part, uniting with it, and forming an interlayer connection type conductor foil tension board, and a process of carrying out wiring patterning of said conductor foil.

[Claim 4]A manufacturing method of the multilayer interconnection board according to claim 3, wherein conductor foil is electrolytic copper foil.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the manufacturing method of a multilayer interconnection board, and relates to the manufacturing method of the multilayer interconnection board which connects between wiring pattern layers from penetrated type beer in more detail.
[0002]
[Description of the Prior Art]Via the insulation layer (layer insulation body layer), generally the hole penetrated to a thickness direction is drilled in an insulation layer, a conductive metal skin is provided in the internal surface of this hole, and electric connection between the wiring pattern layers allocated in lamination and one is made by what is called through hole connection or beer connection. To carry out by being filled up with conductive paste in the breakthrough drilled in the insulation layer is also tried for simplification of an interlayer connection process. Namely, the hole which penetrates a layer insulation body layer (****) is provided in the electric connected part between said wiring pattern layers, Restoration and embedding and forming necessary through hole connection are known in conductive paste in the hole instead of growing up a conductive metal skin into this inner-wall-of-hole side, and forming through hole connection in it.
[0003]For example, in the case of both-sides type patchboard, it is generally manufactured in the following procedures. First, the electrolytic copper foil beforehand formed for the conductive bump (conductive projections) in the prescribed position at the woven glass fabric at the both-principal-planes side of the prepreg layer (glass-epoxy-resin system) which made the epoxy resin impregnate with and adhere, The pile and arrangement of the electrolytic copper foil which has not provided the conductive bump are carried out, heating / application-of-pressure molding is carried out, and a double-sided copper-clad laminate sheet is manufactured.
[0004]Here, the thickness of a prepreg layer and electrolytic copper foil is chosen and set up with the design specification (thickness of a patchboard, circuit pattern width and wiring density) of both-sides type patchboard, etc. In process of said heating / application-of-pressure molding, since resin in the glass-epoxy-resin system prepreg layer which accomplishes a layer insulation body layer takes a plastic stage, a conductive bump's tip part penetrates a prepreg layer, opposite-** to the electrolytic-copper-foil side which counters, and electric connection is formed.
[0005]Then, both-sides type patchboard which has a desired circuit pattern is manufactured by the electrolytic-copper-foil side of a double-sided copper-clad laminate sheet by performing photo etching processing and carrying out wiring patterning.
[0006]On the other hand, in connection with the latest insincere / little-ized tendency, also in the various patchboards containing both-sides type patchboard, insincere-ization etc. are demanded and slimming down of a patchboard, multilayering of wiring, minuteness making of wiring, or densification of wiring is attained.
[0007]
[Problem(s) to be Solved by the Invention]However, in the case of the method which makes through hole connection between wiring pattern layers, fault like the next is accepted by

penetration of the above-mentioned conductive bump's layer insulation body layer. For example, thickness By the specification of about 0.2 mm, even if it chooses and sets up the thickness of a glass-epoxy-resin system prepreg layer (insulation layer) and electrolytic copper foil (conductor layer), we are anxious about the fall of a manufacturing yield by the variation in the quality of these raw materials. There is also a problem of being easy to invite the steep rise of a manufacturing cost by complicated-ization of a manufacturing process and work operation, etc.
[0008]That is, although the size, shape, etc. of the above-mentioned **** vamp are beforehand set up by distribution, layer insulation body layer thickness, etc. of an interlayer connection part, they may produce the faulty connection over the conductor layer side which counters, etc. by the presentation of a layer insulation body layer, or the variation (heterogeneity and heterogeneity) of thickness. And wiring patterning of a next process is performed as what said interlayer connection has accomplished after laminate integration as predetermined. Therefore, beer connection may be insufficient and there is a possibility that the reliability and the yield as a patchboard may be spoiled.
[0009]By the method which performs an interlayer connection to the both principal planes of a core wiring board by a conductive bump in the manufacturing process of the above-mentioned multilayer interconnection board. When multilayering a wiring pattern layer and going, it is difficult for the heat contraction nature of a layer insulation body layer, etc. to influence, and to be easy to produce curvature, if it carries out for every one side, and to obtain a good multilayer interconnection board.
[0010]this invention was looked like [the above-mentioned situation], coped with it, was made, can recognize the connected state between wiring pattern layers visually easily, and aims at offer of the manufacturing method which can obtain a reliable multilayer interconnection board with the sufficient yield.
[0011]
[Means for Solving the Problem]A process at which an invention of claim 1 provides conductive projections in the 1 principal surface of conductor foil, A process of forming in the 1 principal surface of a detachability base material an insulation layer in which thermofusion thru/or heat softening is possible, A process of making an insulation layer countering a conductive-projections forming face of said conductor foil, and carrying out lamination arrangement of the detachability base material, A process which performs heat pressing processing to said layered product, makes a tip part of conductive projections **** and is made to opposite-** melting-izing thru/or a softened insulation layer to a detachability base material side which counters, A process at which a tip part of conductive projections which carry out the strip of said detachability base material, and carry out insulating isolation mutually is exposed, It is a manufacturing method of a multilayer interconnection board having a process of carrying out lamination arrangement of the conductor foil, and performing heat pressing processing to an exposed surface of said conductive-projections tip part, uniting with it, and forming a front-back-connection type conductor foil tension board, and the process of carrying out wiring patterning of said double-sided conductor foil.
[0012]An invention of claim 2 is characterized by conductor foil being electrolytic copper foil in a manufacturing method of the multilayer interconnection board according to claim 1.
[0013]A process at which an invention of claim 3 provides conductive projections in a prescribed position of said circuit pattern of a core wiring board with which a circuit pattern is provided in the at least 1 principal surface, A process of forming in the 1 principal surface of a detachability base material an insulation layer in which thermofusion thru/or heat softening is possible, A process of making an insulation layer countering a conductive-projections forming face of said core wiring board, and carrying out lamination arrangement of the detachability base material, A process which performs heat pressing processing to said layered product, makes a tip part of conductive projections **** and is made to opposite-** melting-izing thru/or a softened insulation layer to a detachability base material side which counters, A process at which a tip part of conductive projections which carry out the strip of said detachability base material, and carry out insulating isolation mutually is exposed, It is a manufacturing method of a multilayer interconnection board having a process of carrying out lamination arrangement of the conductor

foil, and performing heat pressing processing to an exposed surface of said conductive-projections tip part, uniting with it, and forming an interlayer connection type conductor foil tension board, and the process of carrying out wiring patterning of said conductor foil.
[0014]An invention of claim 4 is characterized by conductor foil being electrolytic copper foil in a manufacturing method of the multilayer interconnection board according to claim 3.
[0015]In this invention, as the conductive body, electrolytic copper foil, aluminum foil, etc. about 12-35 micrometers thick are mentioned, for example, and the construction material and thickness are suitably chosen with a use, thickness, etc. of a multilayer interconnection board to manufacture. Core wiring boards are control of thickness of a multilayer interconnection board to manufacture, and a thing which contributes to mechanical intensity, Generally, it is thickness. Are about 0.1-1.0 mm and For example, a glass-epoxy-resin system, A patchboard which made an insulator the sheets (or a film thru/or sheet metal) of a polyimide resin system, a bismaleimide triazine resin system, a phenol resin system, a polyester resin system, a melamine resin system, and a polycarbonate resin system is mentioned.
[0016]In this invention, formation of conductive projections (conductive bump) to the principal surface of conductor foil or a core wiring board, For example, conductive resin paste can be formed by repeating desiccation after screen-stencil and printing suitably using a metal mask conical shape or the shape of a pyramid of a prescribed dimension (a diameter of the bottom, height). A size and shape of the above-mentioned conductive projections are not limited to shape of said illustration. Here, the pastes which mixed conductive powder, such as silver, gold, copper, and solder powder, such after alloy powder or compound (mixing) metal powder, and a resin binder component, for example, and were prepared as conductive resin paste are mentioned.
[0017]As the above-mentioned resin binder component, thermosetting resin, such as ****** plasticity resin, such as polycarbonate resin, polysulfone resin, polyester resin, and phenoxy resin, phenol resin, polyimide resin, and an epoxy resin, etc. are generally mentioned, for example. In addition, a methylmetaacrylate, a diethyl methylmetaacrylate, Trimethylolpropane triacrylate, diethylene-glycol diethyl acrylate, Methyl acrylate, ethyl acrylate, diethyleneglycol ethoxyl acrylate, Ultraviolet curing type resin or electron-beam-irradiation hardening resin, such as acrylic ester, such as acrylate of epsilon-caprolactone denaturation dipentaerythritol, and methacrylic acid ester, etc. is mentioned.
[0018]In this invention, a detachability base material is a relative thing with resin which forms a layer insulation body layer, and copper foil, aluminium foil, etc. which the detachability of a grade which can, in short, transfer a layer insulation body layer is required, for example, have a glossy surface are mentioned. As an insulation layer supported by said detachability base material side, thermoplastics is mentioned, for example and, as for the thickness, about 30-100 micrometers is generally preferred.
[0019]Here, as thermoplastics, sheets, such as 6 4 fluoridation [polycarbonate resin, polysulfone resin, thermoplastic polyimide and polyethylene resin] and polypropylene resin fluoridation and polyether ether ketone resin, are mentioned, for example. As thermosetting resin (prepreg) held at a state before hardening, The sheets of crude rubber, such as an epoxy resin, bismaleimide triazine resin, polyimide resin, phenol resin, polyester resin, melamine resin or butadiene rubber, isobutylene isoprene rubber, crude rubber, neoprene rubber, and silicone rubber, are mentioned. These synthetic resins may be the constituents which could contain an insulating inorganic substance and packing of an organic matter system although it could be independent, and were further combined with reinforcing members, such as glass fabrics, a mat, organic synthesis fiber cloths and a mat, or paper.
[0020]By the invention of claim 1 and claim 2, a conductor layer which a conductor tip part which accomplishes an interlayer connection **** a layer insulation body layer certainly, and forms a wiring pattern layer where it is checked whether fixed flat face-ization for connection has accomplished is arranged and unified. That is, since multilevel interconnection-ization advances checking formation **** of sufficient and reliable interlayer connection, a quality multilayer interconnection board is provided with a sufficient yield.
[0021]In addition to a case of an invention of above-mentioned claim 1-2, in an invention of

claim 3 and claim 4, a circuit pattern by which the interlayer connection was carried out is formed in a field of a core wiring board. That is, since a patchboard which thickness is controlled and specified and guarantees a predetermined mechanical strength beforehand is used as a core and a circuit pattern is formed in this core wiring board side via a layer insulation body layer, a multilayer interconnection board which is fixed thickness mostly and has moderate mechanical intensity is manufactured with a sufficient yield.

[0022]

[Embodiment of the Invention]The following and drawing 1 (a) – (f) And drawing 2 (a) – (h) It is referred to and an example is described.

[0023]Drawing 1 (a) – (f) It is a sectional view showing typically the manufacturing process of the multilayer interconnection board concerning the 1st example.

[0024]First, the conductive paste of a – phenol resin system is screen-stenciled via the metal screen version in the end of silver dust to the prescribed position of the roughened surface of the 35-micrometer-thick electrolytic copper foil 1, and it is drawing 1 (a). It is height abbreviation so that an important section may be shown in section. The 120-micrometer conical shape conductive bump 2 was formed. Here, the metal screen version is a product made from a stainless steel plate about 0.15 mm thick, and it is ** in which the hole of the diameter of about 0.15 mm in thickness was drilled, and the conical shape conductive bump's 2 formation was performed by repeating screen-stencil and desiccation 5 times.

[0025]On the other hand, what applied / formed the epoxy-system-resin semi cure (semi hardened state) layer 3 about 50 micrometers thick in the glossy surface of the 35-micrometer-thick copper foil 4 was prepared. Subsequently, as an important section was shown in drawing 1 (b) in section, the epoxy-system-resin semi cure layer 3 was made to counter conical shape conductive bump 2 forming face of said electrolytic copper foil 1, and lamination arrangement of the copper foil 4 was carried out.

[0026]It is abbreviation about the above-mentioned layered product. It heated at 130 **, the laminator of pressure 1 kgf/cm^2 was passed by feed-rate [of 0.5 m/sec] ., and it unified. By this laminator passage, it is drawing 1 (c). The conductive bump's 2 tip part **** heat softening thru/or the melting-ized epoxy-system-resin semi cure layer 3, and opposite-** it to the glossy surface of the copper foil 4 which counters so that an important section may be shown in section. When the copper foil 4 is exfoliated from said epoxy-system-resin semi cure layer 3 after cooling, it is drawing 1 (d). The copper foil tension board 5 which made the same flat face as the epoxy-system-resin semi cure layer 3, and carried out insulating isolation mutually, and conductive bump 2 tip part exposed was obtained so that an important section might be shown in section. Next, drawing 1 (d) Make a roughened surface counter the conductive bump 2 tip-part exposed surface of said copper foil tension board 5, and heat pressing of 35-micrometer-thick electrolytic-copper-foil 1' is laminated and carried out to it so that an important section may be shown in section, Drawing 1 (e) The electrolytic copper foil 1 as an important section shown in section, and the double-sided copper foil panel 6 which 1' electrically connected by the conductive bamboo 2 were manufactured. Then, to the copper foil 1 of said double-sided copper foil panel 6, and 1' side with screen printing. After printing the necessary etching pattern and carrying out etching removal of the unnecessary part weight foil by using the solution of ferric chloride as an etching reagent, the both-sides type patchboard which has a necessary through hole terminal area was obtained by removing etching KUREJISUTO.

[0027]The patchboard manufactured by the above has a good initial flow, and the connection resistance of a double-side wiring patterned layer, For example When this value took into consideration the pattern resistance (vamp copper-foil-patterns resistance 1-mohm per part per piece) of copper foil by 2.1 ohms, the average of through hole connection resistance was set to 1-mohm, and beer connection resistance and copper-foil-patterns resistance had little variation. The rate of change of the resistance after a solder heat test (288**x10sec.) was also 10% or less.

[0028]Drawing 2 (a) – (h) It is a sectional view showing typically the manufacturing process of the multilayer interconnection board concerning the 2nd example.

[0029]First, drawing 2 (a) It is height like [prepare the core wiring board 8 with which the circuit patterns 7a and 7b were formed in both principal planes as show an important section in section, and / the prescribed position of one circuit pattern 7a] the case of the 1st example of the above. The about 230-micrometer conical shape conductive bump 2 was formed. What applied / formed the epoxy-system-resin semi cure (semi hardened state) layer 3 about 80 micrometers thick in the glossy surface of the 35-micrometer-thick copper foil 4 was prepared.
[0030]Subsequently, drawing 2 (b) The epoxy-system-resin semi cure layer 3 was made to counter conical shape conductive bump 2 forming face of said core wiring board 8, and lamination arrangement of the copper foil 4 was carried out so that an important section might be shown in section.
[0031]It is abbreviation about the above-mentioned layered product. It heated at 110 **, the laminator of pressure 1 kgf/cm^2 was passed by feed-rate [of 0.5 m/sec] ., and it unified. By this laminator passage, it is drawing 2 (c). The conductive bump's 2 tip part **** heat softening thru/or the melting-ized epoxy-system-resin semi cure layer 3, and opposite-** it to the glossy surface of the copper foil 4 which counters so that an important section may be shown in section. After cooling and drawing 2 (d) The conical shape conductive bump 2 is formed in other circuit pattern 7b forming faces of the core wiring board 8, further, the epoxy-system-resin semi cure layer 3 is made for this conical shape conductive bump 2 to counter a forming face, and lamination arrangement of the copper foil 4 is carried out so that an important section may be shown in section. Then, lamination processing is performed like the above and it is drawing 2 (e). If the copper foil 4 of the 3rd page of said both epoxy-system-resin semi cure layer is exfoliated after manufacturing a laminate sheet as an important section shown in section, Drawing 1 (f) Wiring blank 5' which made the same flat face as the epoxy-system-resin semi cure layer 3, and carried out insulating isolation mutually, and conductive bump 2 tip part exposed was obtained so that an important section might be shown in section.
[0032]Next, a roughened surface is made to counter the conductive bump 2 tip-part exposed surface of said wiring blank 5', heat pressing of 35-micrometer-thick electrolytic-copper-foil 1' is laminated and carried out to it, and it is drawing 1 (g). Electrolytic-copper-foil 1' as shows an important section in section manufactured double-sided copper foil panel 6' electrically connected by the conductive bamboo 2. Then, for example by drilling, the breakthrough was drilled in the prescribed position, this drilling inner-wall-of-hole side formed the plating flow to it, and through hole connection was made to it. Subsequently, etching KUREJISUTO is removed, after printing a necessary etching pattern to the both copper foil 1' side of double-sided copper foil panel 6' and carrying out etching removal of the unnecessary part weight foil to it by using the solution of ferric chloride as an etching reagent with screen printing, Drawing 1 (h) The multilayer interconnection board which has the through hole terminal area 9 as shows an important section in section was obtained.
[0033]The patchboard manufactured by the above the connection resistance of the double-side wiring patterned layer, For example When this value took into consideration the pattern resistance (vamp copper-foil-patterns resistance 1-mohm per part per piece) of copper foil by 2.1 ohms, the average of through hole connection resistance was set to 1-mohm, and beer connection resistance and copper-foil-patterns resistance had little variation.
[0034]It was attached to the above-mentioned multilayer interconnection board, and the rate of change of next (260**x20sec.) resistance was also 10% or less.
[0035]This invention is not limited to the above-mentioned example, is a range which does not deviate from the meaning of an invention, and can take various modification. For example, a layer insulation body layer may be thermoplastics instead of epoxy resin system prepreg, and conductive projections can be formed with other conductive compositions other than - phenol resin in the end of silver dust. A core wiring board may be a patchboard which has the interlayer connection manufactured, for example in the 1st example.
[0036]
[Effect of the Invention]According to the invention of claims 1 and 2, since insulating isolation can be carried out and it can check [in / for whether it is derivation **** / a manufacturing

process] to preparation certainly in the field in which the tip part of the conductive projections which form an interlayer connection part forms other circuit patterns, improvement in a manufacturing yield, etc. can be aimed at. In the actual condition that the densification of a multilayer interconnection board, micrifying of an interlayer connection part, etc. are being required especially, it can be called offer of the right manufacturing method.
[0037]according to the invention of claims 3 and 4, the core wiring board side was further used as the base -- a multilayer interconnection board -- since it is-izing, it is easy to control thickness uniformly, and a multilayer interconnection board also with mechanical good intensity can be provided with the sufficient yield.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1](a) (b) (c) (d) (e) (f) Sectional view showing typically the embodiment of the manufacturing method of the multilayer interconnection board concerning the 1st example according to execution order.
[Drawing 2](a) (b) (c) (d) (e) (f) (g) (h) Sectional view showing typically the embodiment of the manufacturing method of the multilayer interconnection board concerning the 2nd example according to execution order.
[Description of Notations]
1 1' .... Electrolytic copper foil
2 .... Conductive projections (conductive bump)
3 .... Insulation layer (epoxy resin system prepreg)
4 .... Detachability base material
5 .... Copper foil panel
5' .... Wiring blank
6 .... Double-sided copper foil panel
7a, 7b .... Circuit pattern
8 .... Core wiring board
9 .... Through hole terminal area

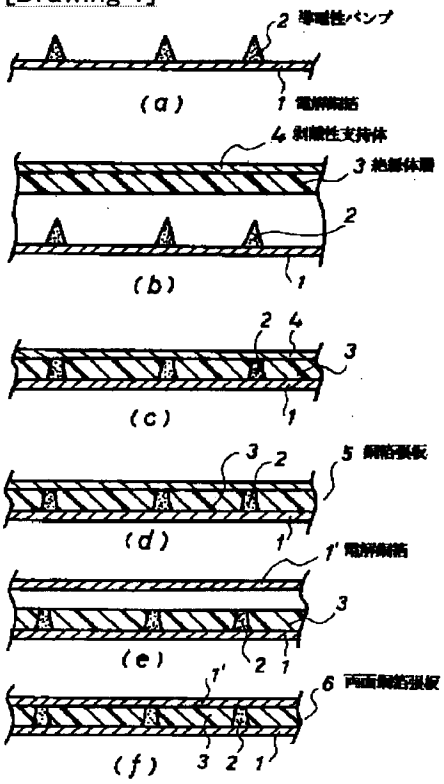
[Translation done.]

* NOTICES *

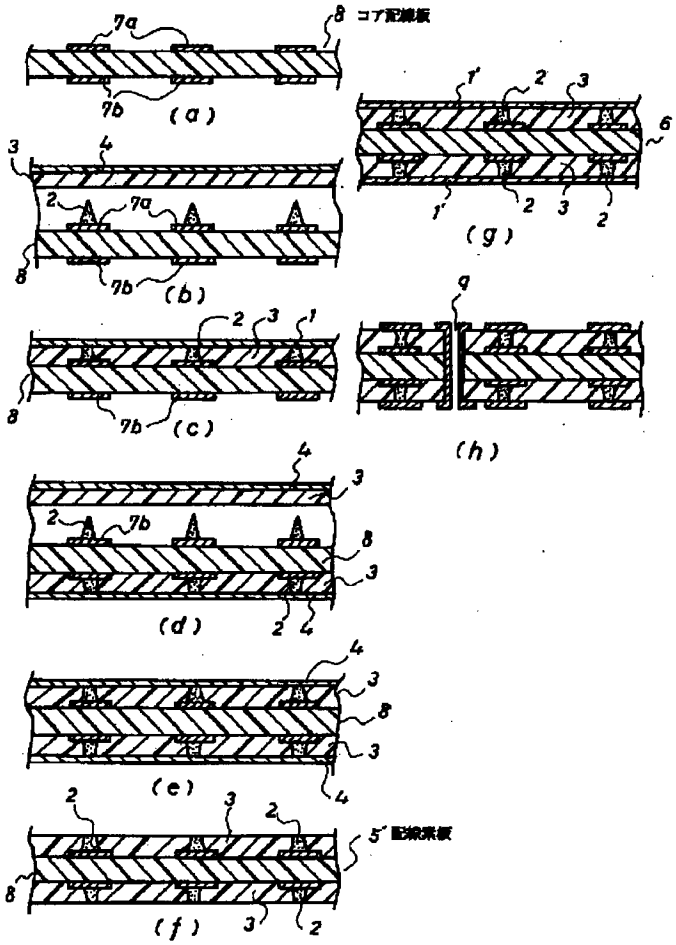
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



[Drawing 2]



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審査請求　未請求　請求項の数４　ＯＬ　（全６頁）

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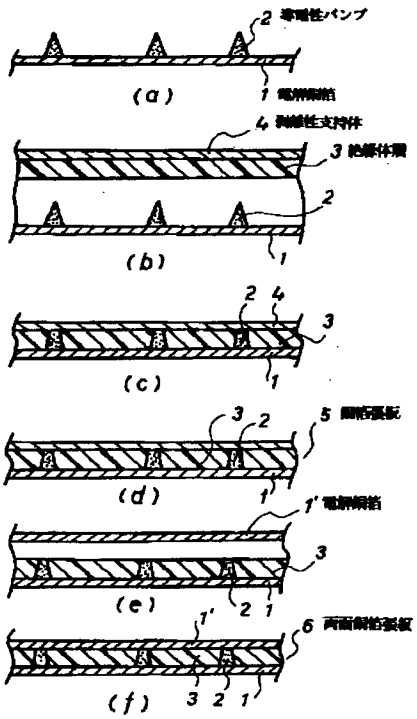
最終頁に続く

(54)【発明の名称】　多層配線板の製造方法

(57)【要約】
【課題】　配線パターン層間の接続状態を容易に視認でき、信頼性の高い多層配線板を歩留まりよく得られる製造方法の提供。
【解決手段】　導電体箔１の一主面に導電性突起２を設ける工程と、剥離性支持体４の一主面に熱溶融ないし熱軟化が可能な絶縁体層３を形成する工程と、前記導電体箔１の導電性突起２形成面に、絶縁体層３を対向させて剥離性支持体４を積層配置する工程と、前記積層体に加熱加圧処理を施し、溶融化ないし軟化した絶縁体層３を導電性突起２の先端部を貫挿させ、対向する剥離性支持体４面に対接させる工程と、前記剥離性支持体４を剥離除去し、互いに絶縁隔離する導電性突起２の先端部を露出させる工程と、前記導電性突起２先端部の露出面に導電体箔１′を積層配置し、加熱加圧処理を施して一体化して両面接続型の導電体箔張り板６を形成する工程と、前記両面導電体箔１，１′を配線パターニングする工程とを有することを特徴とする多層配線板の製造方法である。



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【特許請求の範囲】

【請求項１】　導電体箔の一主面に導電性突起を設ける工程と、

剥離性支持体の一主面に熱溶融ないし熱軟化が可能な絶縁体層を形成する工程と、

前記導電体箔の導電性突起形成面に、絶縁体層を対向させて剥離性支持体を積層配置する工程と、

前記積層体に加熱加圧処理を施し、溶融化ないし軟化した絶縁体層を導電性突起の先端部を貫挿させ、対向する剥離性支持体面に対接させる工程と、

前記剥離性支持体を剥離除去し、互いに絶縁隔離する導電性突起の先端部を露出させる工程と、

前記導電性突起先端部の露出面に導電体箔を積層配置し、加熱加圧処理を施して一体化して両面接続型の導電体箔張り板を形成する工程と、

前記両面導電体箔を配線パターニングする工程と、を有することを特徴とする多層配線板の製造方法。

【請求項２】　導電体箔が電解銅箔であることを特徴とする請求項１記載の多層配線板の製造方法。

【請求項３】　少なくとも一主面に配線パターンが設けられているコア配線板の、前記配線パターンの所定位置に導電性突起を設ける工程と、

剥離性支持体の一主面に熱溶融ないし熱軟化が可能な絶縁体層を形成する工程と、

前記コア配線板の導電性突起形成面に、絶縁体層を対向させて剥離性支持体を積層配置する工程と、

前記積層体に加熱加圧処理を施し、溶融化ないし軟化した絶縁体層を導電性突起の先端部を貫挿させ、対向する剥離性支持体面に対接させる工程と、

前記剥離性支持体を剥離除去し、互いに絶縁隔離する導電性突起の先端部を露出させる工程と、

前記導電性突起先端部の露出面に導電体箔を積層配置し、加熱加圧処理を施して一体化して層間接続型の導電体箔張り板を形成する工程と、

前記導電体箔を配線パターニングする工程と、を有することを特徴とする多層配線板の製造方法。

【請求項４】　導電体箔が電解銅箔であることを特徴とする請求項３記載の多層配線板の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、多層配線板の製造方法に係り、さらに詳しくは配線パターン層間を貫通型ビアで接続する多層配線板の製造方法に関する。

【０００２】

【従来の技術】絶縁体層（層間絶縁体層）を介し、積層・一体的に配設された配線パターン層間の電気的な接続は、一般的に、絶縁体層に厚さ方向に貫通する孔を穿設し、この孔の内壁面に導電性のメッキ層を設け、いわゆるスルホール接続もしくはビア接続で行っている。また、層間接続工程の簡略化のため、絶縁体層に穿設した

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貫通孔内に、導電性ペーストを充填して行うことも試みられている。すなわち、前記配線パターン層間の電気的な接続箇所に、層間絶縁体層を貫通（貫挿）する孔を設け、この孔内壁面に導電性のメッキ層を成長させ、スルホール接続を形成する代りに、孔内に導電性ペーストを充填・埋め込み、所要のスルホール接続を形成することが知られている。

【０００３】たとえば、両面型配線板の場合は、一般的に、次のような手順で製造されている。先ず、ガラス布にエポキシ樹脂を含浸・付着させた（ガラス・エポキシ樹脂系）プリプレグ層の両主面側に、予め、所定位置に導電性バンプ（導電性突起）を設けてある電解銅箔と、導電性バンプを設けてない電解銅箔とを重ね・配置し、加熱・加圧成型して両面銅張り積層板を製造する。

【０００４】ここで、プリプレグ層および電解銅箔の厚さは、両面型配線板の設計仕様（配線板の厚さ、配線パターン幅・配線密度）などによって選択・設定される。また、前記加熱・加圧成型の過程で、層間絶縁体層を成すガラス・エポキシ樹脂系プリプレグ層中の樹脂は、軟化溶融状態を採るので、導電性バンプの先端部がプリプレグ層を貫通し、対向する電解銅箔面に対接して電気的な接続が形成される。

【０００５】その後、両面銅張り積層板の電解銅箔面に、フォトエッチング処理を施して配線パターニングすることにより、所望の配線パターンを有する両面型配線板が製造される。

【０００６】一方、最近の軽薄・短小化傾向に伴って、両面型配線板を含む各種配線板においても、軽薄化などが要求されており、配線板の薄型化、配線の多層化、配線の微細化ないし配線の高密度化などが図られている。

【０００７】

【発明が解決しようとする課題】しかしながら、上記導電性バンプの層間絶縁体層の貫通によって、配線パターン層間のスルホール接続を行う方式の場合、次ぎのような不具合が認められる。たとえば、厚さ 0.2mm程度の仕様で、ガラス・エポキシ樹脂系プリプレグ層（絶縁体層）および電解銅箔（導電体層）の厚さを選択・設定しても、それら素材の品質のバラツキによって、製造歩留まりの低下が懸念される。また、製造工程・作業操作の煩雑化などによって、製造コストの大幅なアップを招来し易いなどの問題もある。

【０００８】すなわち、上記電性バンプの寸法・形状などは、層間接続部の分布や層間絶縁体層の厚さなどによって予め設定されるが、層間絶縁体層の組成や厚さのバラツキ（不均質・不均一性）により、対向する導電体層面に対する接続不良などを生じることもある。そして、積層・一体化後においては、前記層間接続が所定通りに成されているものとして、次工程の配線パターニングが行われる。したがって、ビア接続が不十分な場合もあって、配線板としての信頼性や歩留まりが損なわれる恐れ

がある。

【０００９】なお、上記多層配線板の製造工程において、たとえばコア配線板の両主面に、導電性バンプによって層間接続を行う方式で、配線パターン層を多層化して行くとき、片面ごとに行う層間絶縁体層の熱収縮性などが影響して反りが生じ易く、良質な多層配線板を得ることが困難である。

【００１０】本発明は、上記事情に対処してなされたもので、配線パターン層間の接続状態を容易に視認でき、信頼性の高い多層配線板を歩留まりよく得られる製造方法の提供を目的とする。

【００１１】

【課題を解決するための手段】請求項１の発明は、導電体箔の一主面に導電性突起を設ける工程と、剥離性支持体の一主面に熱溶融ないし熱軟化が可能な絶縁体層を形成する工程と、前記導電体箔の導電性突起形成面に、絶縁体層を対向させて剥離性支持体を積層配置する工程と、前記積層体に加熱加圧処理を施し、溶融化ないし軟化した絶縁体層を導電性突起の先端部を貫挿させ、対向する剥離性支持体面に対接させる工程と、前記剥離性支持体を剥離除去し、互いに絶縁隔離する導電性突起の先端部を露出させる工程と、前記導電性突起先端部の露出面に導電体箔を積層配置し、加熱加圧処理を施して一体化して両面接続型の導電体箔張り板を形成する工程と、前記両面導電体箔を配線パターニングする工程とを有することを特徴とする多層配線板の製造方法である。

【００１２】請求項２の発明は、請求項１記載の多層配線板の製造方法において、導電体箔が電解銅箔であることを特徴とする。

【００１３】請求項３の発明は、少なくとも一主面に配線パターンが設けられているコア配線板の、前記配線パターンの所定位置に導電性突起を設ける工程と、剥離性支持体の一主面に熱溶融ないし熱軟化が可能な絶縁体層を形成する工程と、前記コア配線板の導電性突起形成面に、絶縁体層を対向させて剥離性支持体を積層配置する工程と、前記積層体に加熱加圧処理を施し、溶融化ないし軟化した絶縁体層を導電性突起の先端部を貫挿させ、対向する剥離性支持体面に対接させる工程と、前記剥離性支持体を剥離除去し、互いに絶縁隔離する導電性突起の先端部を露出させる工程と、前記導電性突起先端部の露出面に導電体箔を積層配置し、加熱加圧処理を施して一体化して層間接続型の導電体箔張り板を形成する工程と、前記導電体箔を配線パターニングする工程とを有することを特徴とする多層配線板の製造方法である。

【００１４】請求項４の発明は、請求項３記載の多層配線板の製造方法において、導電体箔が電解銅箔であることを特徴とする。

【００１５】本発明において、導電性体としては、たとえば厚さ12～35μｍ程度の電解銅箔やアルミ箔などが挙げられ、その材質および厚さは、製造する多層配線板の

用途や厚さなどによって適宜選択する。また、コア配線板は、製造する多層配線板の厚さの制御、および機械的な強度に寄与するものであり、一般的に、厚さ 0.1～1.0mm程度であり、たとえばガラス・エポキシ樹脂系、ポリイミド樹脂系、ビスマレイミドトリアジン樹脂系、フェノール樹脂系、ポリエステル樹脂系、メラミン樹脂系、ポリカーボネート樹脂系のシート類（もしくはフィルムないし薄板）などを絶縁体とした配線板が挙げられる。

【００１６】本発明において、導電体箔やコア配線板の主面に対する導電性突起（導電性バンプ）の形成は、たとえばメタルマスクを用い、導電性樹脂ペーストをスクリーン印刷、印刷後の乾燥を適宜繰り返すことによって、所定寸法（底面径，高さ）の円錐状もしくは角錐状に形成できる。なお、上記導電性突起の大きさ・形状は、前記例示の形状に限定されない。ここで、導電性樹脂ペーストとしては、たとえば銀，金，銅，半田粉などの導電性粉末、これらの合金粉末もしくは複合（混合）金属粉末と、樹脂バインダー成分とを混合して調製されたペースト類が挙げられる。

【００１７】なお、上記樹脂バインダー成分としては、たとえばポリカーボネート樹脂、ポリスルホン樹脂、ポリエステル樹脂、フェノキシ樹脂などの熱可過塑性樹脂、フェノール樹脂、ポリイミド樹脂、エポキシ樹脂などの熱硬化性樹脂などが一般的に挙げられる。その他、メチルメタアクリレート、ジエチルメチルメタアクリレート、トリメチロールプロパントリアクリレート、ジエチレングリコールジエチルアクリレート、アクリル酸メチル、アクリル酸エチル、アクリル酸ジエチレングリコールエトキシレート、ε－カプロラクトン変性ジペンタエリスリトールのアクリレートなどのアクリル酸エステル、メタアクリル酸エステルなどの紫外線硬化型樹脂もしくは電子線照射硬化型樹脂などが挙げられる。

【００１８】本発明において、剥離性支持体は、層間絶縁体層を形成する樹脂との相対的なもので、要するに層間絶縁体層を転写できる程度の剥離性が要求され、たとえば光沢面を有する銅箔、アルミニウム箔などが挙げられる。また、前記剥離性支持体面に担持される絶縁体層としては、たとえば熱可塑性樹脂が挙げられ、その厚さは、一般的に、30～ 100μｍ 程度が好ましい。

【００１９】ここで、熱可塑性樹脂としては、たとえばポリカーボネート樹脂、ポリスルホン樹脂、熱可塑性ポリイミド樹脂、４フッ化ポリエチレン樹脂、６フッ化ポリプロピレン樹脂、ポリエーテルエーテルケトン樹脂などのシート類が挙げられる。また、硬化前の状態に保持される熱硬化性樹脂（プリプレグ）としては、エポキシ樹脂、ビスマレイミドトリアジン樹脂、ポリイミド樹脂、フェノール樹脂、ポリエステル樹脂、メラミン樹脂、あるいはブタジェンゴム、ブチルゴム、天然ゴム、ネオプレンゴム、シリコーンゴムなどの生ゴムのシート

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類が挙げられる。これら合成樹脂は、単独でもよいが絶縁性無機物や有機物系の充填物を含有してもよく、さらにガラスクロスやマット、有機合成繊維布やマット、あるいは紙などの補強材と組み合わせた組成物であってもよい。

【００２０】請求項１および請求項２の発明では、層間接続を成す導電体先端部が、層間絶縁体層を確実に貫挿し、かつ一定の接続用平坦面化が成されているか否かが確認された状態で、配線パターン層を形成する導電体層を配置・一体化する。つまり、十分かつ信頼性の高い層間接続の形成可能を確認しながら、多層配線化が進行されるため、高品質な多層配線板が歩留まりよく提供される。

【００２１】請求項３および請求項４の発明では、上記請求項１～２の発明の場合に加え、コア配線板の面に層間接続された配線パターンが形成される。つまり、予め、厚さが制御・規定され、かつ所定の機械的強度を保証する配線板をコアとし、このコア配線板面に層間絶縁体層を介して配線パターンが形成されるため、ほぼ一定厚で、かつ適度の機械的な強度を有する多層配線板が歩留まりよく製造される。

【００２２】

【発明の実施の形態】以下、図１(a) ～(f) および図２(a) ～(h) を参照して実施例を説明する。

【００２３】図１(a) ～(f) は、第１の実施例に係る多層配線板の製造工程を模式的に示す断面図である。

【００２４】先ず、厚さ35μm の電解銅箔１の粗化面の所定位置に、メタルスクリーン版を介して、銀粉末－フェノール樹脂系の導電性ペーストをスクリーン印刷して、図１(a) に要部を断面的に示すごとく、高さ約 120μm の円錐状導電性バンプ２を形成した。ここで、メタルスクリーン版は、厚さ約0.15mmのステンレス鋼板製で、厚さ約0.15mm径の孔が穿設されたもであり、また、円錐状導電性バンプ２の形成は、スクリーン印刷および乾燥を５回繰り返して行った。

【００２５】一方、厚さ約50μm 程度のエポキシ系樹脂セミキュア（半硬化状態）層３を厚さ35μm の銅箔４の光沢面に塗布／形成したものを用意した。次いで、図１(b)に要部を断面的に示すごとく、前記電解銅箔１の円錐状導電性バンプ２形成面に、エポキシ系樹脂セミキュア層３を対向させて銅箔４を積層配置した。

【００２６】上記積層体を約 130℃に加熱し、圧力1kgf／cm² のラミネータを送り速度0.5m／sec.で通過させて一体化した。このラミネータ通過により、図１(c) に要部を断面的に示すごとく、導電性バンプ２の先端部は、熱軟化ないし溶融化したエポキシ系樹脂セミキュア層３を貫挿し、対向する銅箔４の光沢面に対接する。冷却後、前記エポキシ系樹脂セミキュア層３から銅箔４を剥離すると、図１(d) に要部を断面的に示すごとく、エポキシ系樹脂セミキュア層３と同一平坦面をなし、かつ互

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いに絶縁隔離して導電性バンプ２先端部が露出した銅箔張り板５を得た。次に、図１(d) に要部を断面的に示すごとく、前記銅箔張り板５の導電性バンプ２先端部露出面に、粗化面を対向させて厚さ35μm の電解銅箔１′ を積層し、加熱加圧して、図１(e) に要部を断面的に示すような、電解銅箔１，１′ が導電性バンプ２で電気的に接続した両面銅箔張板６を製造した。その後、前記両面銅箔張板６の銅箔１，１′ 面にスクリーン印刷法で、所要のエッチングパターンを印刷し、塩化第二鉄の水溶液をエッチング液として不要部分銅箔をエッチング除去してから、エッチンクレジストを除去することにより、所要のスルホール接続部を有する両面型の配線板を得た。

【００２７】上記によって製造した配線板は、初期導通が良好であり、両面配線パターン層の接続抵抗は、たとえば 2.1Ω で、この値は、銅箔のパターン抵抗（バンプ1個当たりの銅箔パターン抵抗分1mΩ）を考慮すると、スルホール接続抵抗の平均が1mΩとなって、ビア接続抵抗および銅箔パターン抵抗ともバラツキが少ないものであった。また、半田耐熱試験（ 288℃×10sec.）後における抵抗値の変化率も10%以下であった。

【００２８】図２(a) ～(h) は、第２の実施例に係る多層配線板の製造工程を模式的に示す断面図である。

【００２９】先ず、図２(a) に要部を断面的に示すような、両主面に配線パターン7a，7bが設けられたコア配線板８を用意し、一方の配線パターン7aの所定位置に、上記第１の実施例の場合と同様にして、高さ 230μm 程度の円錐状導電性バンプ２を形成した。また、厚さ約80μm 程度のエポキシ系樹脂セミキュア（半硬化状態）層３を厚さ35μm の銅箔４の光沢面に塗布／形成したものを用意した。

【００３０】次いで、図２(b) に要部を断面的に示すごとく、前記コア配線板８の円錐状導電性バンプ２形成面に、エポキシ系樹脂セミキュア層３を対向させて銅箔４を積層配置した。

【００３１】上記積層体を約 110℃に加熱し、圧力1kgf／cm² のラミネータを送り速度0.5m／sec.で通過させて一体化した。このラミネータ通過により、図２(c) に要部を断面的に示すごとく、導電性バンプ２の先端部は、熱軟化ないし溶融化したエポキシ系樹脂セミキュア層３を貫挿し、対向する銅箔４の光沢面に対接する。冷却後、図２(d) に要部を断面的に示すごとく、コア配線板８の他の配線パターン7b形成面に、円錐状導電性バンプ２を形成し、さらに、この円錐状導電性バンプ２を形成面に、エポキシ系樹脂セミキュア層３を対向させて銅箔４を積層配置する。　その後、上記と同様にラミネート処理を行い、図２(e) に要部を断面的に示すような、積層板を製造してから、前記両エポキシ系樹脂セミキュア層３面の銅箔４を剥離すると、図１(f) に要部を断面的に示すごとく、エポキシ系樹脂セミキュア層３と同一平坦面をなし、かつ互いに絶縁隔離して導電性バンプ２先

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端部が露出した配線素板５′を得た。

【００３２】次に、前記配線素板５′の導電性バンプ２先端部露出面に、粗化面を対向させて厚さ35μｍの電解銅箔１′を積層し、加熱加圧して、図１(g)に要部を断面的に示すような、電解銅箔１′が導電性バンプ２で電気的に接続した両面銅箔張板６′を製造した。その後、所定位置に、たとえばドリル加工によって貫通孔を穿設し、この穿設孔内壁面のメッキ導通化し、スルホール接続を行った。次いで、両面銅箔張板６′の両銅箔１′面にスクリーン印刷法で、所要のエッチングパターンを印刷し、塩化第二鉄の水溶液をエッチング液として不要部分銅箔をエッチング除去してから、エッチンクレジストを除去して、図１(h)に要部を断面的に示すような、スルホール接続部９を有する多層配線板を得た。

【００３３】上記によって製造した配線板は、その両面配線パターン層の接続抵抗は、たとえば 2.1Ωで、この値は、銅箔のパターン抵抗（バンプ 1個当たりの銅箔パターン抵抗分1mΩ）を考慮すると、スルホール接続抵抗の平均が1mΩとなって、ビア接続抵抗および銅箔パターン抵抗ともバラツキが少ないものであった。

【００３４】また、上記多層配線板につき、（ 260℃×20sec.）後における抵抗値の変化率も10%以下であった。

【００３５】なお、本発明は、上記実施例に限定されるものでなく、発明の趣旨を逸脱しない範囲で、いろいろの変形を採ることができる。たとえば層間絶縁体層は、エポキシ樹脂系プリプレグの代りに、熱可塑性樹脂であってもよいし、また、導電性突起は銀粉末－フェノール樹脂以外の他の導電性組成物で形成することができる。さらに、コア配線板は、たとえば第１の実施例で製造した層間接続を有する配線板であってもよい。

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【００３６】

【発明の効果】請求項１，２の発明によれば、層間接続部を形成する導電性突起の先端部が他の配線パターンを形成する面に、確実に、また絶縁隔離して導出いるかを製造工程において、用意に確認することができるので、製造歩留まりの向上など図ることができる。特に、多層配線板の高密度化、層間接続部の微小化などが要求されつつある現状において、当を得た製造方法の提供といえる。

【００３７】請求項３，４の発明によれば、さらに、コア配線板面をベースとした多層配線板化であるため、厚さを一定に制御し易いし、また機械的な強度も良好な多層配線板を歩留まりよく提供できる。

【図面の簡単な説明】

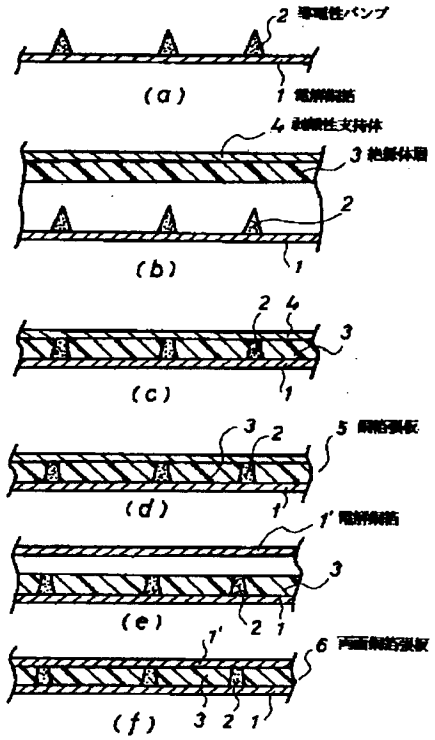
【図１】(a)，(b)，(c)，(d)，(e)，(f)は第１の実施例に係る多層配線板の製造方法の実施態様を実施順に従い模式的に示す断面図。

【図２】(a)，(b)，(c)，(d)，(e)，(f)，(g)，(h)は第２の実施例に係る多層配線板の製造方法の実施態様を実施順に従い模式的に示す断面図。

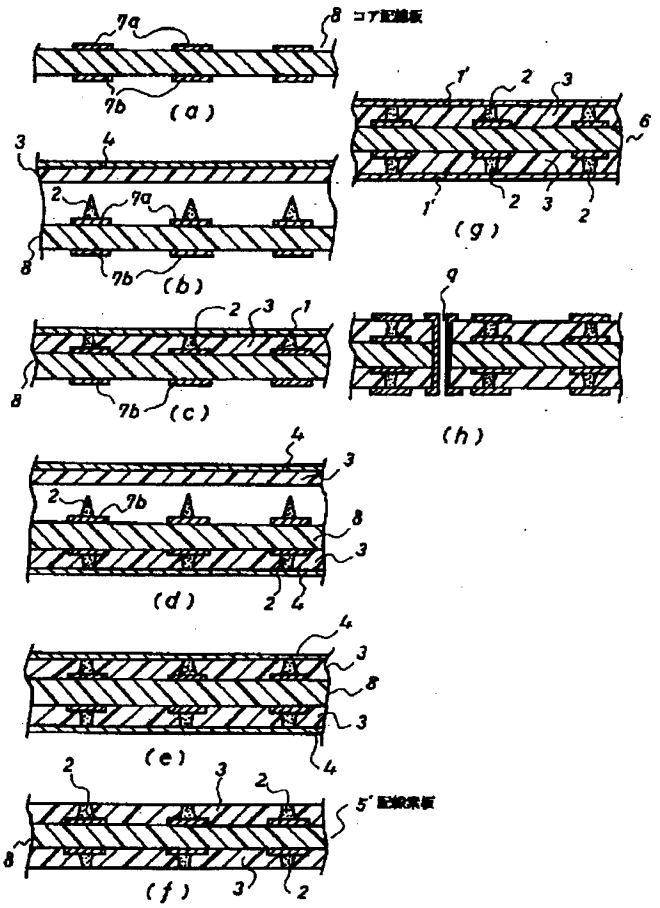
【符号の説明】

１，１′……電解銅箔
２……導電性突起（導電性バンプ）
３……絶縁体層（エポキシ樹脂系プリプレグ）
４……剥離性支持体
５……銅箔張板
５′……配線素板
６……両面銅箔張板
7a，7b……配線パターン
８……コア配線板
９……スルホール接続部

【図１】



【図２】



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